**SIRIUS FT TEST PLAN GUIDE (ANALOG PART)**

# Revision History

|  |  |  |  |
| --- | --- | --- | --- |
| Version | Date | Author | Note |
| V0.1 | 2017/09/13 | Yuan.yuan,  Zhe.li | Initial Version |
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## Analog FT plan related pins description

For analog related pin description, please refer to the table 1:

TABLE 1 Sirius Analog part pins description

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Sirius analog part pin description, total pin number=25 | | | | |
| Pin Number | IN/OUT | Ball Name | Description | Pad name |
| A24 | OUT | XTAL2 | Crystal pad2. | XTAL2 |
| B24 | IN | XTAL1 | Crystal pad1, or clock input pad, 20M clk input | XTAL1 |
| F20 | IN | CLKREF\_SEL\_PAD | External clock frequency select 0:40MHz,1:20MHz | CLKREF\_SEL\_PAD |
| H20, H21 | IN | AVSS\_A | ABB analog ground | AVSS |
| J20, J21 | IN | AVDD1V8\_A | ABB analog 1.8V supply | AVDD |
| G19 | IN | AVDD1V8\_OSC | Crystal analog 1.8V power | AVDD\_OSC |
| G20 | IN | AVSS\_OSC | Crystal analog ground | AVSS\_OSC |
| K21 | IN | AVDD1V8\_PLL | ABB PLL analog 1.8V power | AVDD\_PLL |
| K20 | IN | AVSS\_PLL | ABB PLL analog ground | AVSS\_PLL |
| E23 | IN | AD\_IN\_0 | SAR3 input analog signal path 0 | SAR10\_IN\_3[0] |
| E22 | IN | AD\_IN\_1 | SAR3 input analog signal path 1 | SAR10\_IN\_3[1] |
| G21 | IN | AD\_IN\_2 | SAR3 input analog signal path 2 | SAR10\_IN\_3[2] |
| E21 | IN | AD\_IN\_3 | SAR3 input analog signal path 3 | SAR10\_IN\_3[3] |
| F21 | IN | AD\_IN\_4 | SAR3 input analog signal path 4 | SAR10\_IN\_3[4] |
| D21 | IN | AD\_IN\_5 | SAR3 input analog signal path 5 | SAR10\_IN\_3[5] |
| D20 | IN | AD\_IN\_6 | SAR3 input analog signal path 6 | SAR10\_IN\_3[6] |
| C20 | IN | AD\_IN\_7 | SAR3 input analog signal path 7 | SAR10\_IN\_3[7] |
| D26 | IN | RSSI\_1 | A channel RSSI input | SAR10\_IN\_1[0] |
| C25 | IN | PDET\_A\_2G | A channel power detector for 2G carrier | SAR10\_IN\_1[1] |
| D24 | IN | PDET\_B\_2G | A channel power detector for 2G carrier | SAR10\_IN\_1[2] |
| C23 | IN | RSSI\_2 | B channel RSSI input | SAR10\_IN\_2[0] |
| C24 | IN | PDET\_A\_5G | A channel power detector for 5G carrier | SAR10\_IN\_2[1] |
| D23 | IN | PDET\_B\_5G | A channel power detector for 5G carrier | SAR10\_IN\_2[2] |
| A25 | OUT | QDAC\_OUTN\_A | QDAC negative output path A | QDAC\_OUTN\_A |
| B25 | OUT | QDAC\_OUTP\_A | QDAC positive output path A | QDAC\_OUTP\_A |
| B26 | OUT | IDAC\_OUTP\_A | IDAC positive output path A | IDAC\_OUTP\_A |
| A26 | OUT | IDAC\_OUTN\_A | IDAC negative output path A | IDAC\_OUTN\_A |
| A27 | IN | IADC\_VINN\_A | IADC negative input path A | IADC\_VINN\_A |
| C26 | IN | IADC\_VINP\_A | IADC positive input path A | IADC\_VINP\_A |
| B27 | IN | QADC\_VINP\_A | QADC positive input path A | QADC\_VINP\_A |
| B28 | IN | QADC\_VINN\_A | QADC negative input path A | QADC\_VINN\_A |
| C28 | IN | QADC\_VINN\_B | QADC negative input path B | QADC\_VINN\_B |
| C27 | IN | QADC\_VINP\_B | QADC positive input path B | QADC\_VINP\_B |
| D27 | IN | IADC\_VINP\_B | IADC positive input path B | IADC\_VINP\_B |
| D28 | IN | IADC\_VINN\_B | IADC negative input path B | IADC\_VINN\_B |
| E28 | OUT | IDAC\_OUTN\_B | IDAC negative output path B | IDAC\_OUTN\_B |
| E27 | OUT | IDAC\_OUTP\_B | IDAC positive output path B | IDAC\_OUTP\_B |
| F27 | OUT | QDAC\_OUTP\_B | QDAC positive output path B | QDAC\_OUTP\_B |
| F28 | OUT | QDAC\_OUTN\_B | QDAC negative output path B | QDAC\_OUTN\_B |
| E26 | IN | IADC\_VINN\_C | IADC negative input path C | IADC\_VINN\_C |
| E25 | IN | IADC\_VINP\_C | IADC positive input path C | IADC\_VINP\_C |
| F25 | IN | QADC\_VINP\_C | QADC positive input path C | QADC\_VINP\_C |
| F26 | IN | QADC\_VINN\_C | QADC negative input path C | QADC\_VINN\_C |
| F27 | IN | QADC\_VINN\_D | QADC negative input path D | QADC\_VINN\_D |
| H27 | IN | QADC\_VINP\_D | QADC positive input path D | QADC\_VINP\_D |
| G27 | IN | IADC\_VINP\_D | IADC positive input path D | IADC\_VINP\_D |
| G28 | IN | IADC\_VINN\_D | IADC negative input path D | IADC\_VINN\_D |
| G13 | IN | CA7\_AVDD1V8 | A7 PLL analog 1.8V power | A7\_AVDD |
| H13 | IN | CA7\_AVSS1V8 | A7 PLL analog ground | A7\_AVSS |
| AB13 | IN | CEVA\_AVDD1V8 | CEVA PLL analog 1.8V power | CEVA\_AVDD |
| AB14 | IN | CA7\_AVSS1V8 | CEVA PLL analog ground | CEVA\_AVSS |
| G12 | IN | DDR\_AVDD1V8 | DDR PLL analog 1.8V power | DDR\_AVDD18 |
| H12 | IN | DDR\_AVSS1V8 | DDR PLL analog ground | DDR\_AVSS |

### SPI Configuration Guide

## Analog IP FT load board requirements

The analog related tests include:

1. Analog voltage test.

2. PLL frequency test.

3. DACs (4 identical DACs) test.

4. ADCs (total 11 ADCs, with 8 identical and 3 other ADCs) test.

5. Temperature Sensor (TS) test.

6. PVT Sensor test.

The analog input signal frequency is less than 10M, output signal frequency is less than 5M, clock frequency is less than 50M.

The DAC-ADC loop tests need relay and spectrum. The DACs test also need spectrum to perform FFT, whose accuracy is higher than 62dB.

The TS test requires one commercial TS sensor each site to provide reference temperature. TS test results will store into OTP.

1. Analog DC voltage test.

### Analog DC voltage test requirement

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Analog DC voltage/current need to be tested | | | | | |
| Pin Number | Pin Name | Signal Name | Value | Tolerance (%) | SPI configuration |
| D21 | AD\_IN\_5 | VBG | 1.25V | 10 | 1.2.1 |
| PMU\_IOUT | 40uA |  |
| AVDDL\_LDO | 0.9V |  |
| OSC\_LDO | 1.3V |  |
| DAC\_LOCAL\_BIAS\_A | 10uA |  |
| DAC\_LOCAL\_BIAS\_B | 10uA |  |
| ADC\_A\_REFP | 1.35v |  |
| ADC\_A\_REF\_CM | 1.1v |  |
| ADC\_A\_REFN | 0.85v |  |
| ADC\_B\_REFP | 1.35v |  |
| ADC\_B\_REF\_CM | 1.1v |  |
| ADC\_B\_REFN | 0.85v |  |
| ADC\_C\_REFP | 1.35v |  |
| ADC\_C\_REF\_CM | 1.1v |  |
| ADC\_C\_REFN | 0.85v |  |
| ADC\_D\_REFP | 1.35v |  |
| ADC\_D\_REF\_CM | 1.1v |  |
| ADC\_D\_REFN | 0.85v |  |
| DVDD\_LDO | 0.9V |  |
| SAR\_VREF\_1 | 1.25V |  |
| SAR\_VREF\_2 | 1.25V |  |
| SAR\_VREF\_3 | 1.25V |  |
|  |  |  |

TABLE 1.1

* 1. SPI configuration

#### 1.2.1 VBG Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

TABLE 1.2.1

#### 1.2.2 PMU\_IOUT Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

TABLE 1.2.2

#### 1.2.3 AVDDL\_LDO Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

TABLE 1.2.3

#### 1.2.4 OSC\_LDO Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

TABLE 1.2.4

#### 1.2.5 DAC\_LOCAL\_BIAS\_A Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

TABLE 1.2.5

#### 1.2.6 DAC\_LOCAL\_BIAS\_B Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

TABLE 1.2.6

#### 1.2.7 ADC\_A\_REFP Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

TABLE 1.2.7

#### 1.2.8 ADC\_A\_REF\_CM Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

TABLE 1.2.8

#### 1.2.9 ADC\_A\_REFN Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

TABLE 1.2.9

#### 1.2.10 ADC\_B\_REFP Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

TABLE 1.2.10

#### 1.2.11 ADC\_B\_REF\_CM Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

TABLE 1.2.11

#### 1.2.12 ADC\_B\_REFN Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

TABLE 1.2.12

#### 1.2.13 ADC\_C\_REFP Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

TABLE 1.2.13

#### 1.2.14 ADC\_C\_REF\_CM Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

TABLE 1.2.14

#### 1.2.15 ADC\_C\_REFN Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

TABLE 1.2.15

#### 1.2.16 ADC\_D\_REFP Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

TABLE 1.2.16

#### 1.2.17 ADC\_D\_REF\_CM Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

TABLE 1.2.17

#### 1.2.18 ADC\_D\_REFN Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

TABLE 1.2.18

#### 1.2.19 DVDD\_LDO Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

TABLE 1.2.19

#### 1.2.20 SAR\_VREF\_1 Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

TABLE 1.2.20

#### 1.2.21 SAR\_VREF\_2 Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

TABLE 1.2.21

#### 1.2.22 SAR\_VREF\_3 Test

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

TABLE 1.2.22

1. PLL frequency test.

There are total 10 PLLs in Sirius: ADDAPLL, DSPPLL0, DSPPLL1, DSPPLL2, SDCPLL, AUPLL, PIXPLL, A7PLL, CEVAPLL and DDRPLL. The topology is shown in the figure below.

Fig 2.1 Sirius clock test diagram

### 2.1 PLL frequency test

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Pad Number | Pad Name | Signal Name | Value (MHz) | Tolerance (%) | Note |
|  | AD\_IN\_4 | SAR10\_IN\_3[4] | 20 | 1 | ADDAPLL CLKDIV 20MHz |
| 15.625 | 1 | DSPPLL0  2G/128=15.625M |
| 11.71875 | 1 | DSPPLL1  1.5G/128=11.71875M |
| 4.6875 | 1 | DSPPLL2  600M/128=4.6875M |
| 12.5 | 1 | SDCPLL  50M/4=12.5M |
| 5 | 1 | AUPLL  40M\*32/256=5M |
| 18.5625 | 2 | PIXPLL  74.25/4=18.5625MHz |
|  | DE1\_PAD | DE1 | 3.90625 | 1 | A7PLL  500M/128=3.90625M |
|  | PCLK1\_PAD | PCLK1 | 3.90625 | 1 | CEVAPLL  500M/128=3.90625M |
|  | QE1\_3\_PAD | QE1\_3 | 16.65625 | 2 | DDRPLL  533/32=16.65625MHz |

TABLE 2.1

* 1. SPI configuration

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
|  |  |  |  |
|  |  |  |  |

TABLE 2.2

1. DAC-ADC loop test

3.1 DAC-ADC loop test description

We will use the build-in sine-wave generator’s output as DAC’s 12bit input data. The DACs outputs will be a 2MHz single-tone sine waveform. And in load board we need to connect DAC’s output first to a filter whose -3dB corner is 10MHz, and filter order should be larger than 3th. Then filter output should pass a relay, relay’s one output could be connect to spectrum to observe DAC’s output spectrum. And the other output should connect to another relay. This relay can also select input from signal generator. The output connect to relay and finally to ADCA/ADCB or ADCC/ADCD. We have internal FFT processor to compute the ADC output ‘s SNR, THD, SNDR, and we can also mux one channel ADC’s output to monitor pin and use logic analyzer to analyze the data. The loop SNR should be >52dB.

Figure 3 shows the test bench for loop test.



Figure 3 Sirius DA/AD loop Test Bench

### 3.2 SPI configuration

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

TABLE 3.2

### 3.3 DACs test requirements

The following table shows the DACs test output requirements.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| DAC test output requirements | | | | |
| Number | Name | Value | Tolerance (%) | Note |
| 1 | Peak-to-Peak output swing | 0.5V | 15 | Differential value (when using the first way to test ).Refer to 3.5 |
| 2 | Peak-to-Peak output swing | 1V | 15 | Differential value (when using the second way to test ). Refer to 3.5 |
| 3 | SNDR | >50db |  | fout=2MHz, differential |
| 4 | IQ mismatch | 0 | 9 | Refer to 3.5 |
| 5 | Output common-mode voltage | 0.9V | 15 | The common-mode voltage at each DAC outputs. |
| 6 | Output DC offset | <15mV |  | Differential dc value, use test 5 result to generate:  Vdc\_off=Vcm+-Vcm- |
| 7 | Q\_DAC Peak to peak output swing | 535mV | +-7 | Q path sine wave Vpp Value |

TABLE 3.3

### 3.4 DAC Test Related Pins

|  |  |
| --- | --- |
| Pin Name | Test Value Expression |
| QDAC\_OUTN\_A | V1 |
| QDAC\_OUTP\_A | V2 |
| IDAC\_OUTP\_A | V3 |
| IDAC\_OUTN\_A | V4 |
| IDAC\_OUTN\_B | V15 |
| IDAC\_OUTP\_B | V16 |
| QDAC\_OUTP\_B | V17 |
| QDAC\_OUTN\_B | V18 |

TABLE 3.4

### 3.5 DAC test definition

|  |  |  |
| --- | --- | --- |
| Name | Expression | Definition |
| Peak-to-Peak output swing | Vpp\_Q\_A | Max(V2-V1­)-Min(V2-V1­) |
| Vpp\_I\_A | Max(V3-V4­)-Min(V3-V4­) |
| Vpp\_Q\_B | Max(V17-V18­)-Min(V17-V18­) |
| Vpp\_I\_B | Max(V16-V15­)-Min(V16-V15­) |
| IQ\_mismatch | MA | 1-Vpp\_I\_A/ Vpp\_Q\_A |
| MB | 1-Vpp\_I\_B/ Vpp\_Q\_B |

TABLE 3.5

### 3.6 ADC test requirements

The following table shows the ADCs test output requirements.

|  |  |  |  |
| --- | --- | --- | --- |
| 12 bit ADC test input and output requirements | | | |
| Number | Name | Value | Tolerance (%) |
| 1 | Input frequency | 9MHz | 10 |
| 2 | Input signal common-mode voltage value | 0.9V | 10 |
| 3 | Input signal differential peak-to-peak voltage | 1.4V | 10 |
| 4 | ADC output code peak-to-peak swing | 896 | 15 |
| 5 | ADC output code SNDR | >50dB |  |

TABLE 3.6

* 1. SPI configuration

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

TABLE 3.7

## 4 SAR ADC test

SAR1/SAR2/SAR3 is single-ended 10-bit ADC, whose sampling rate is 100/11MHz. The outputs are denoted as D0~D9, where D9 is the MSB and D0 is the LSB. This SAR ADC only can be tested in DC voltage input case, and output data be read in register.

### 4.1 SPI configuration

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |
| WR |  |  |  |

### 4.2 SAR ADC test requirement

The following table shows the test input and output requirements for the 8-bit ADC (ADC5).

|  |  |  |
| --- | --- | --- |
| Input dc voltage(V) | Output code | Tolerant |
| 0 |  | 0<=delta<=5 |
| 0.625 |  | -7<=delta<=+7 |
| 1.25 |  | -10<=delta<=0 |
|  | 0<=delta<=+10 |
| 1.875 |  | -15<=delta<=+15 |
| 2.5 |  | -20<=delta<=0 |

## 5 TS test.

The calibration principle of Temperature Sensor (TS) is to find out the precise temperature drift, store it in effuse and then compensate it in software stage.

### 5.1 Load Board Requirement

To perform FT calibration, a commercial temperature sensor is required to place near the test site to provide reference temperature. For multi-Site load board design, the placement of commercial TSs are suggested to avoid cross heating, as Fig 5.1 shown.

Please use high accuracy commercial TS products such as **ADT7420/7320 (require I2C or SPI interface, see Appendix I)** for temperature reference.



Fig 5.1 Commercial TS placement suggestion in multi-site load board

### 5.2 FT procedure and SPI configuration

|  |  |  |  |
| --- | --- | --- | --- |
| WR/RD | Address | Data | Note |
|  |  |  | Commercial TS on loadboard keep working |
|  |  | 0 | Set TS\_CLK to 781.25K, TS\_PD=0, TS\_EN=1 |
|  |  | 0 | Wait 50us and readout TS\_DOUT09<8:0>, repeat 4 times and take average code as D\_avg.  Calculate **T\_ate=0.4825\*D\_avg-77.7** |
|  |  | 0 | Readout average commercial TS temperature (at least 4 times average), denoted as T\_ext;), T\_os=T\_ate-T\_ext+16 and store into effuse[4:0] (Please refer to OTP plan for specific bit location) |
|  |  | 0 | If T\_os<0 or T\_os > 31, mark this chip as failed chip and discard it. |
|  |  | 0 | Please also save total current on AVDD18 and DVDD (whole chip current during this IP test) in log file for leakage check. |

## 6 PVT sensor test

Directly read PVT sensor output 16bit code from SPI and compare to ideal code.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| WR/RD | Address | Data | Tolerance (%) | Ideal value |
|  |  |  |  |  |
|  |  |  |  |  |

## Appendix I

**ADT8420 data sheet:**

http://www.analog.com/media/cn/technical-documentation/data-sheets/ADT7420\_cn.pdf